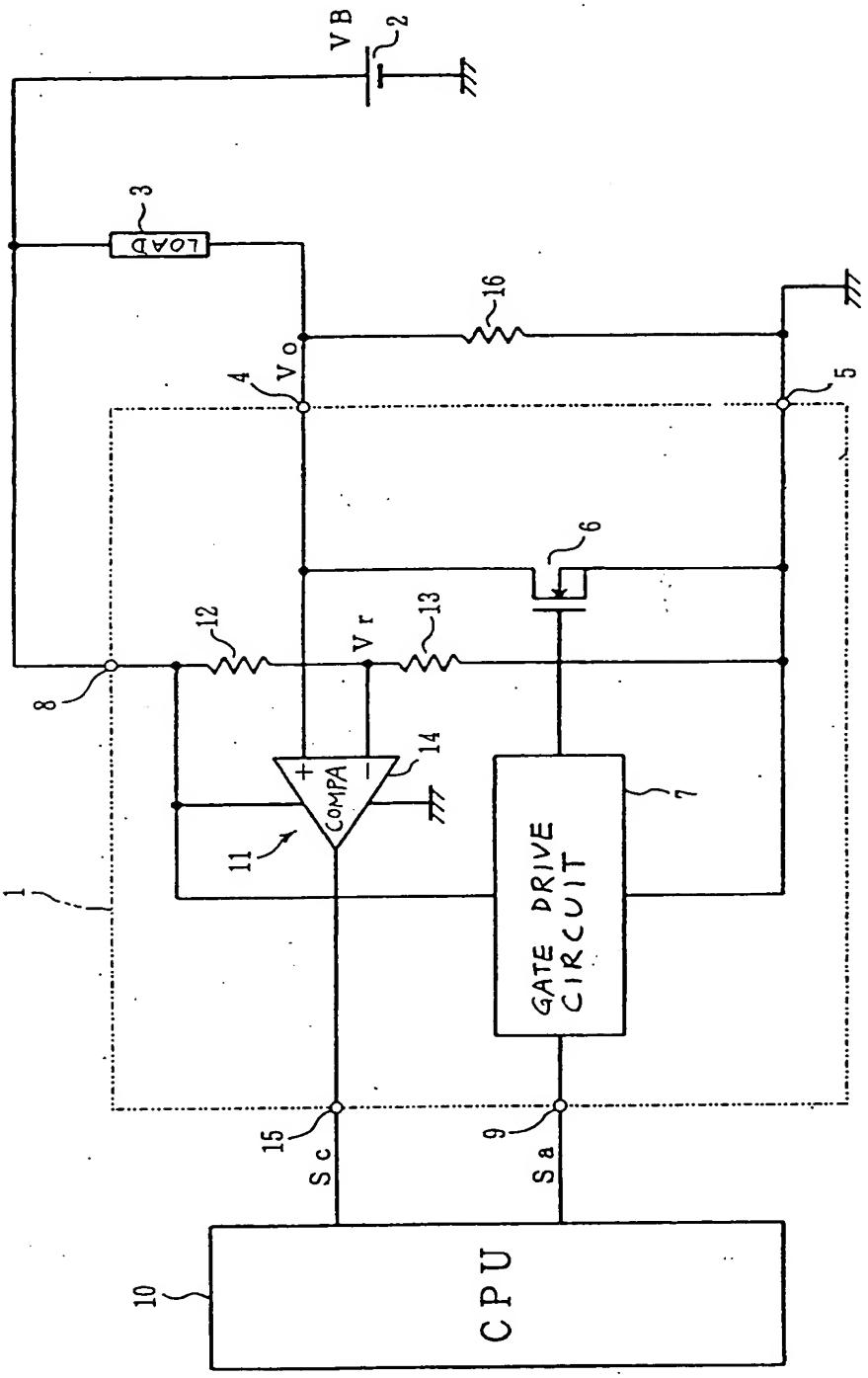


FIG. 1 PRIOR ART

original

FIG. 2

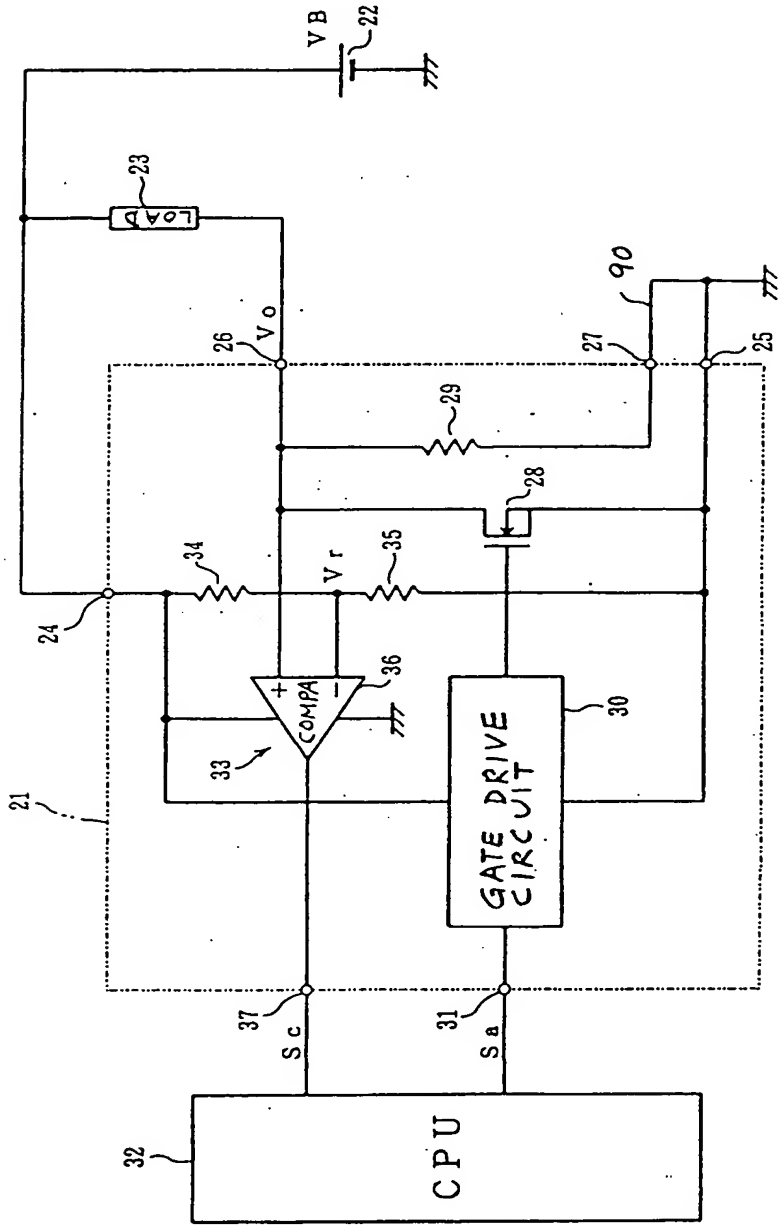

VB
22
23
LOAD
90
26
Vo
27
25
29
28
34
Vr
35
24
36
COMPA
33
21
GATE DRIVE CIRCUIT
30
37
Sc
31
Sa
CPU
32

FIG. 3

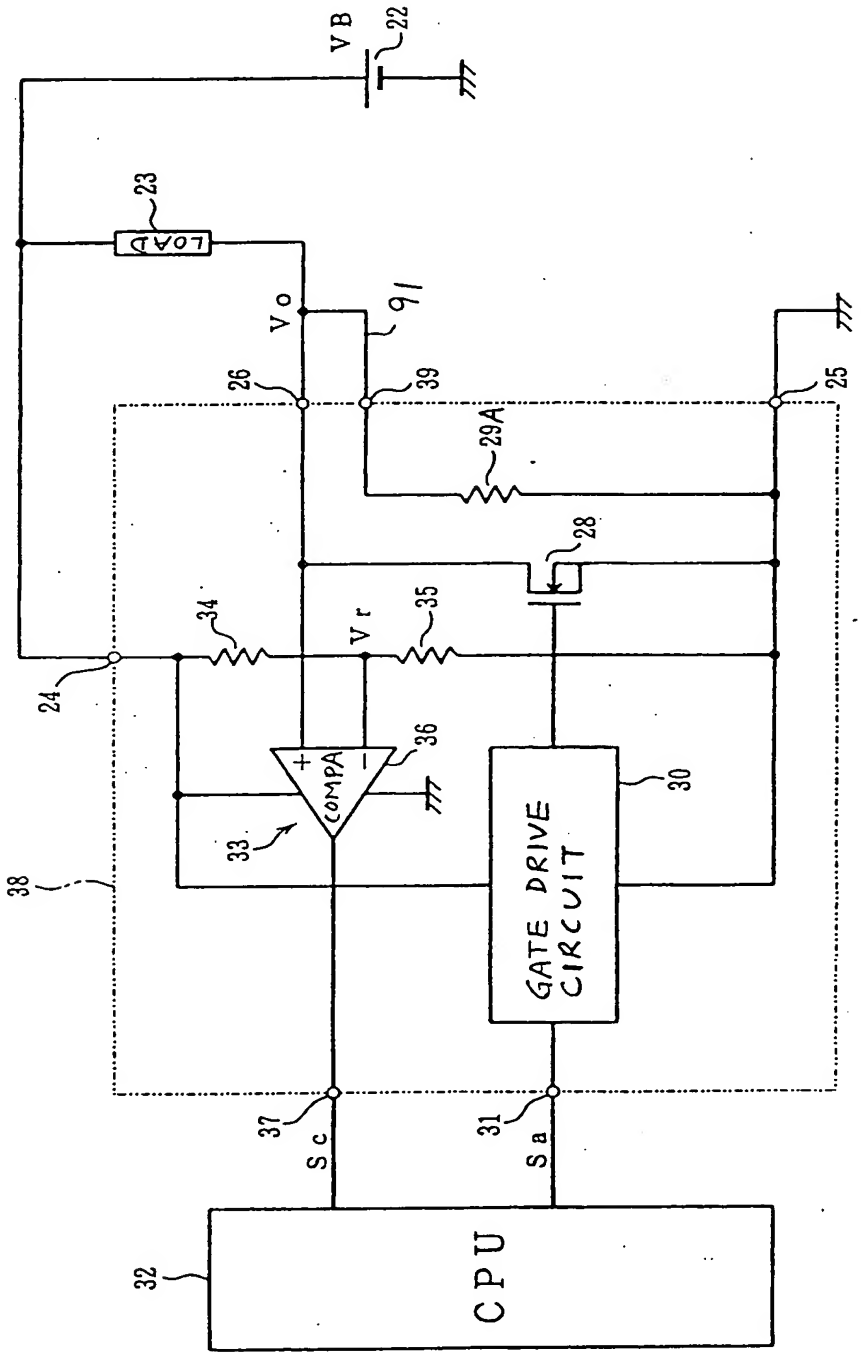

VB
22
23
LOAD
Vo
91
26
39
25
29A
28
34
Vr
35
24
+
COMPA
−
36
33
38
GATE DRIVE CIRCUIT
30
37
Sc
31
Sa
CPU
32

FIG. 4

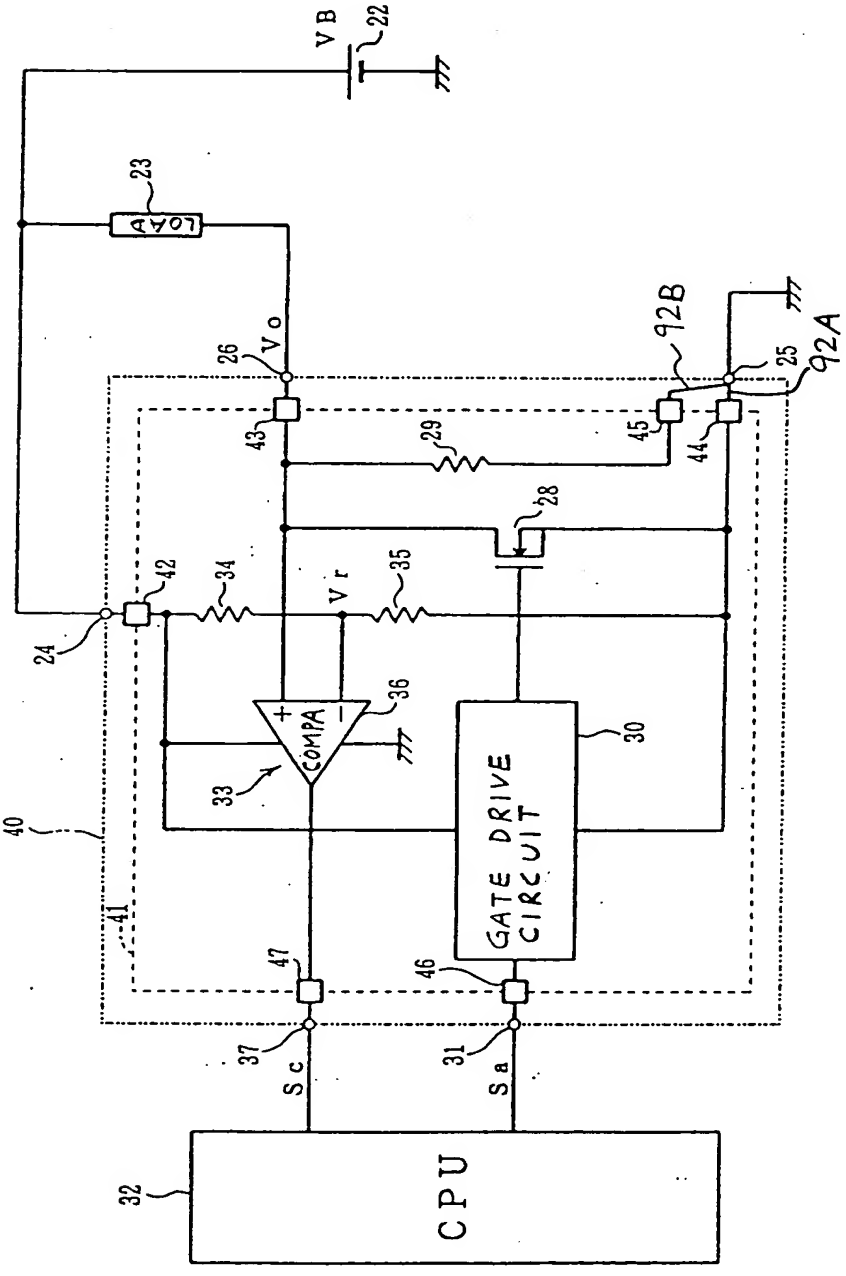

VB
22
23
LOAD
26
Vo
92B
92A
25
43
45
44
29
28
42
34
Vr
35
24
36
COMPA
33
30
GATE DRIVE CIRCUIT
40
41
47
46
37
Sc
31
Sa
CPU
32

FIG. 5

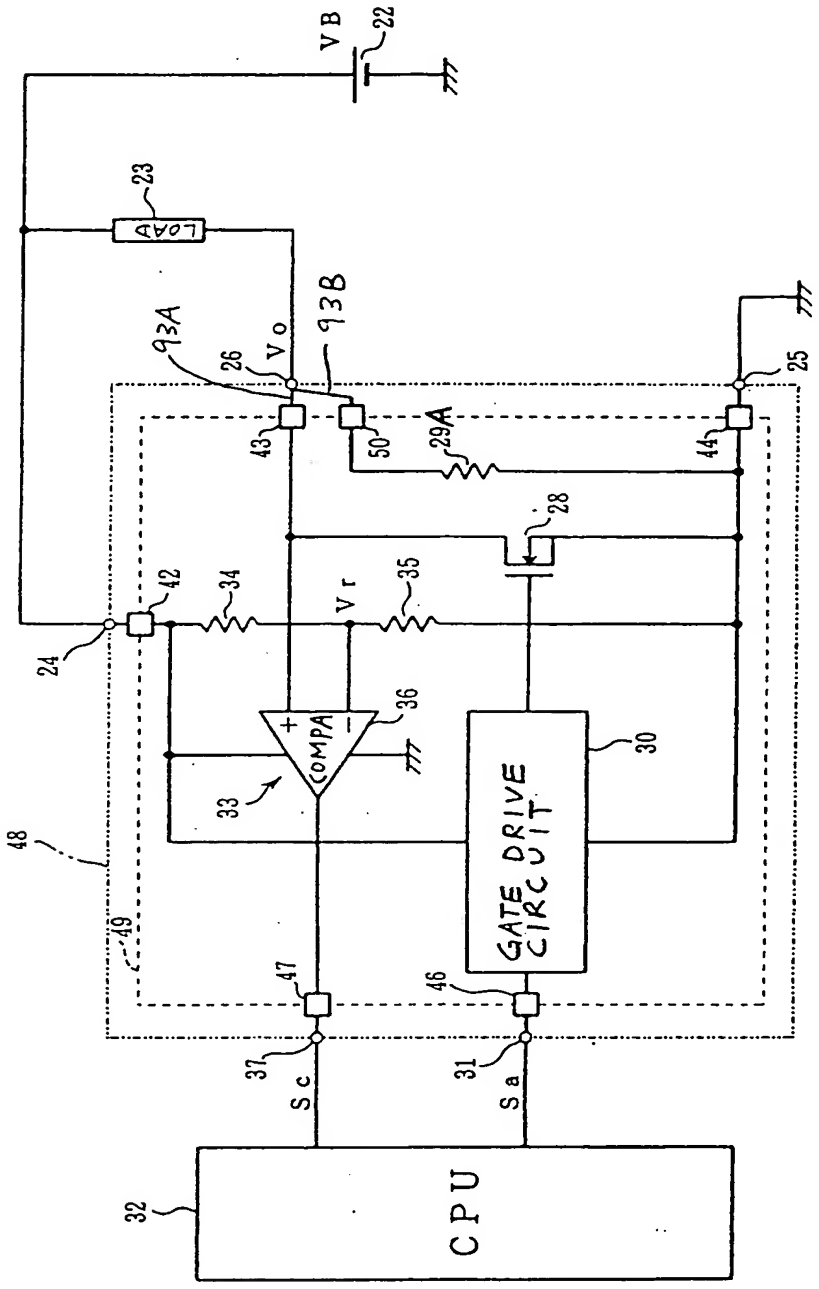

VB
22
23
LOAD
93A
93B
26
Vo
25
43
50
29A
44
28
42
34
Vr
35
24
36
COMPA
33
30
GATE DRIVE CIRCUIT
48
49
47
46
37
Sc
31
Sa
CPU
32

FIG. 6

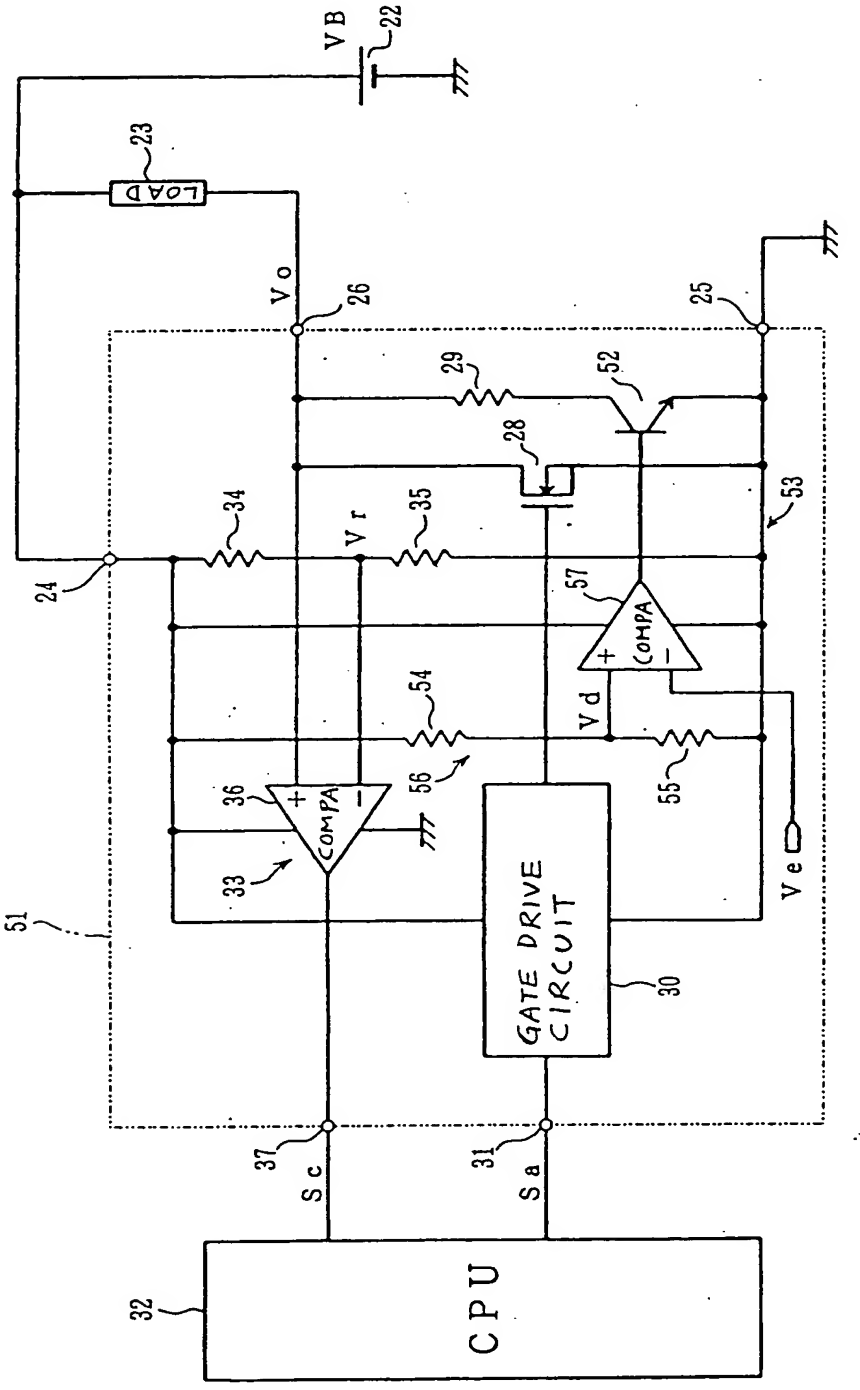

VB
22
23
LOAD
Vo
26
25
29
52
28
34
Vr
35
53
24
57
COMPA
54
Vd
55
56
36
COMPA
33
51
GATE DRIVE CIRCUIT
30
Ve
37
Sc
31
Sa
CPU
32

FIG. 7

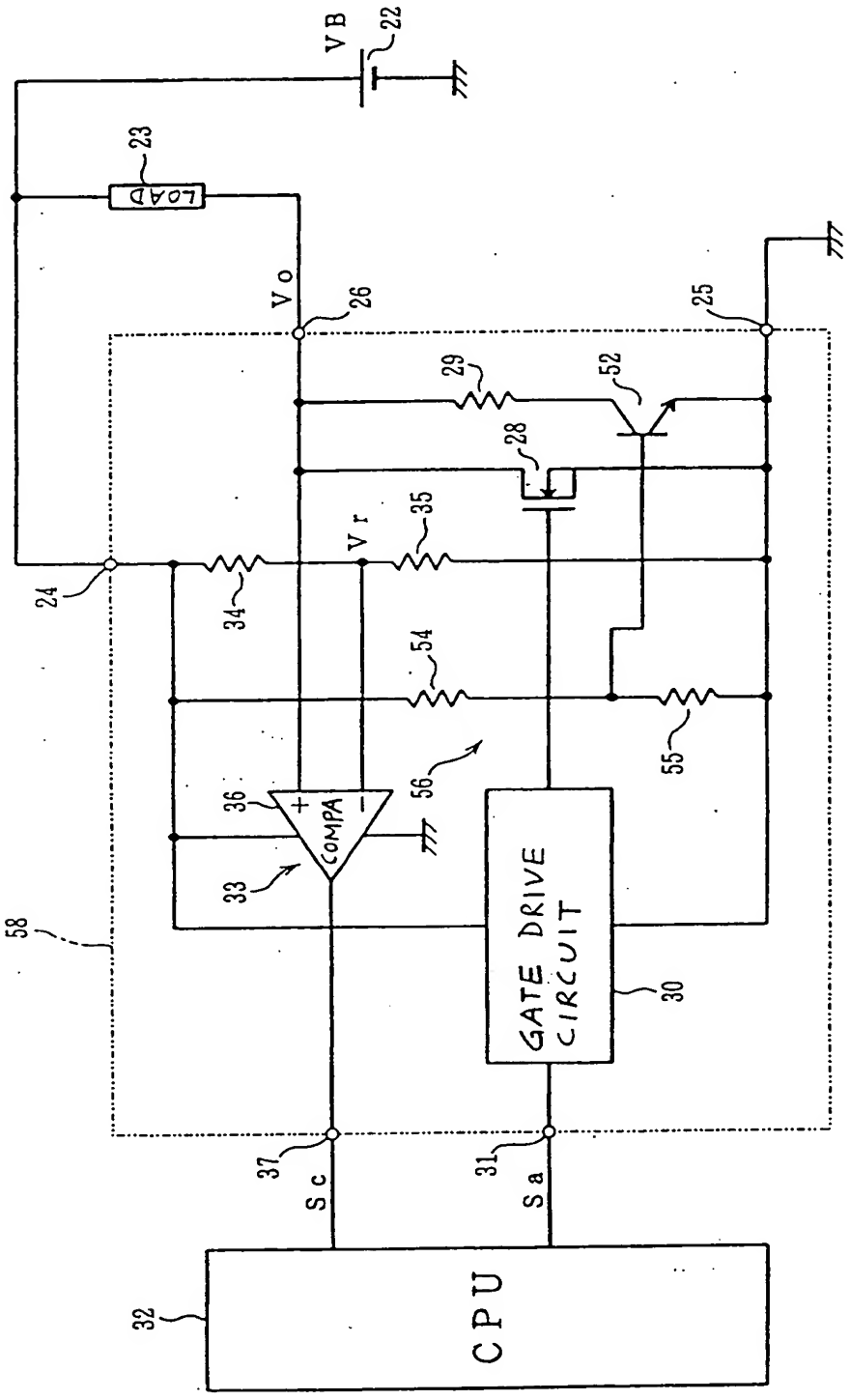
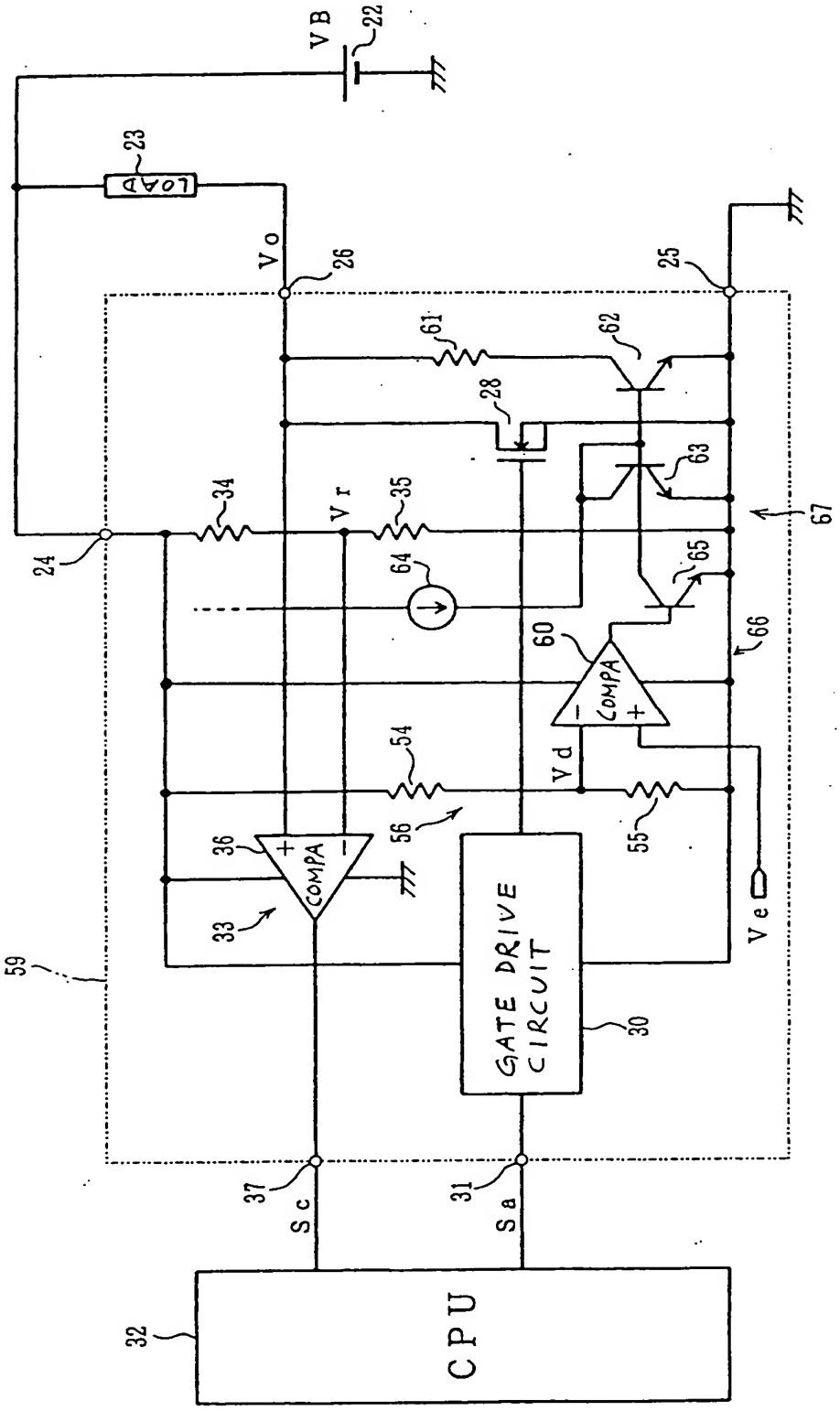

VB
22
23
LOAD
Vo
26
25
29
52
28
Vr
35
24
34
54
55
56
36
COMPA
33
58
GATE DRIVE CIRCUIT
30
37
Sc
31
Sa
CPU
32

FIG. 8


VB
22
23
LOAD
Vo
26
25
61
62
28
63
34
Vr
35
67
24
64
65
66
60
COMPA
54
Vd
55
56
36
COMPA
33
59
GATE DRIVE CIRCUIT
30
Ve
37
Sc
31
Sa
CPU
32

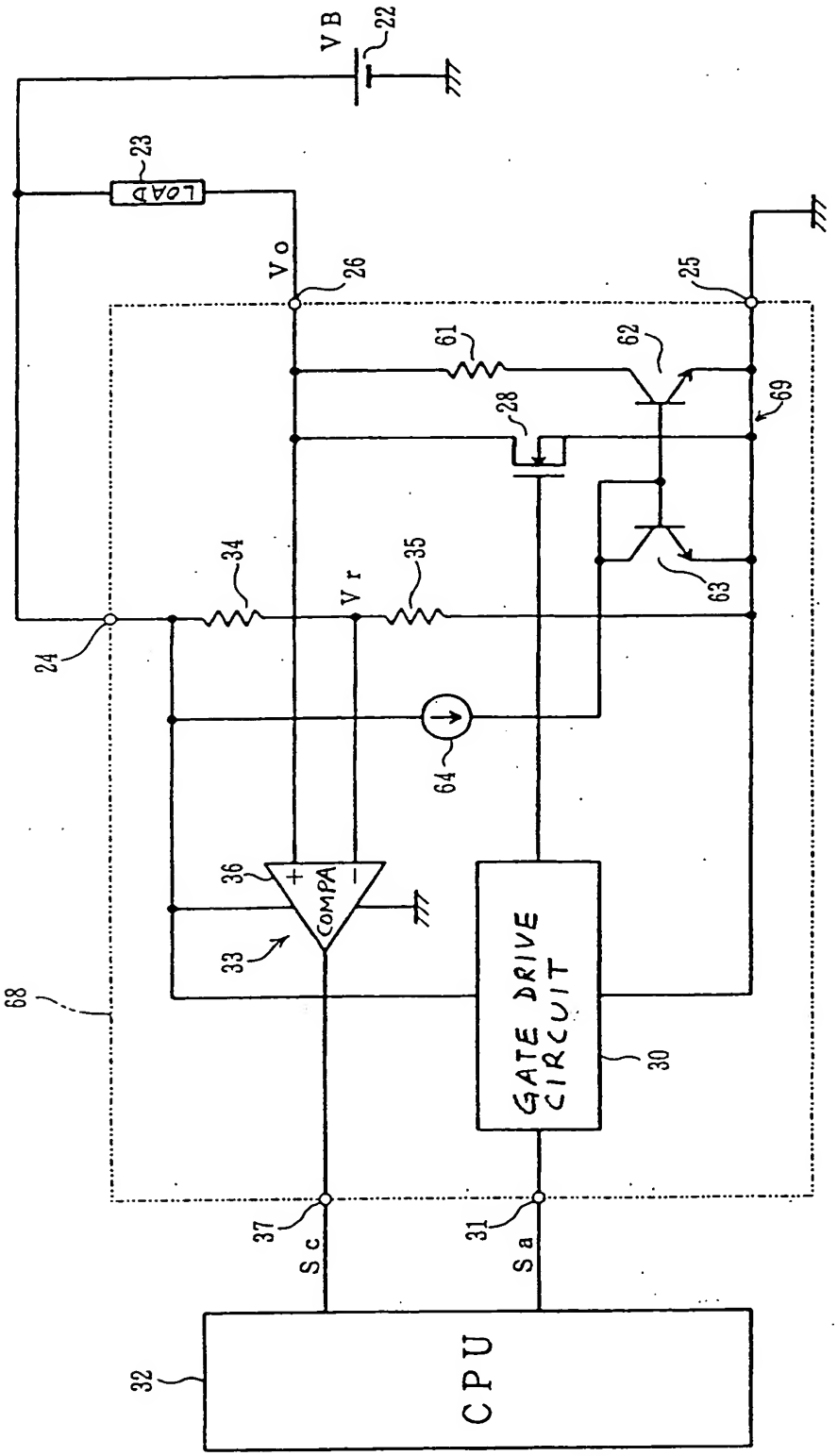

VB
22
23
LOAD
Vo
26
25
61
62
69
28
34
Vr
35
63
24
64
36
COMPA
33
68
GATE DRIVE CIRCUIT
30
37
Sc
31
Sa
CPU
32

FIG. 9